

SDRAM
1M x 16 Bit x 4 Banks
FEATURES

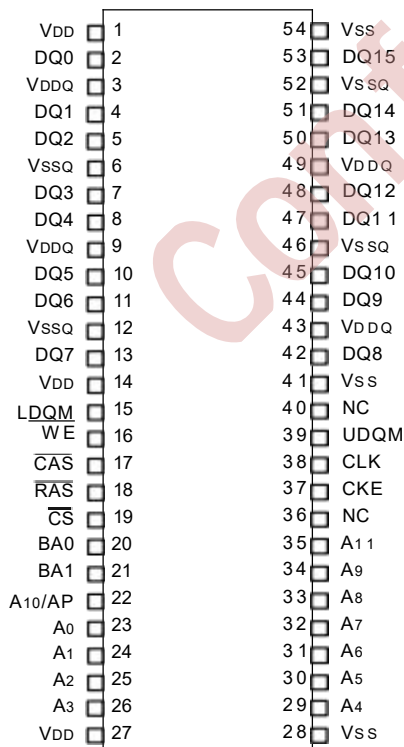
- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS Latency (2 & 3)
 - Burst Length (1, 2, 4, 8 & full page)
 - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)
 - 15.6 μ s refresh interval

ORDERING INFORMATION

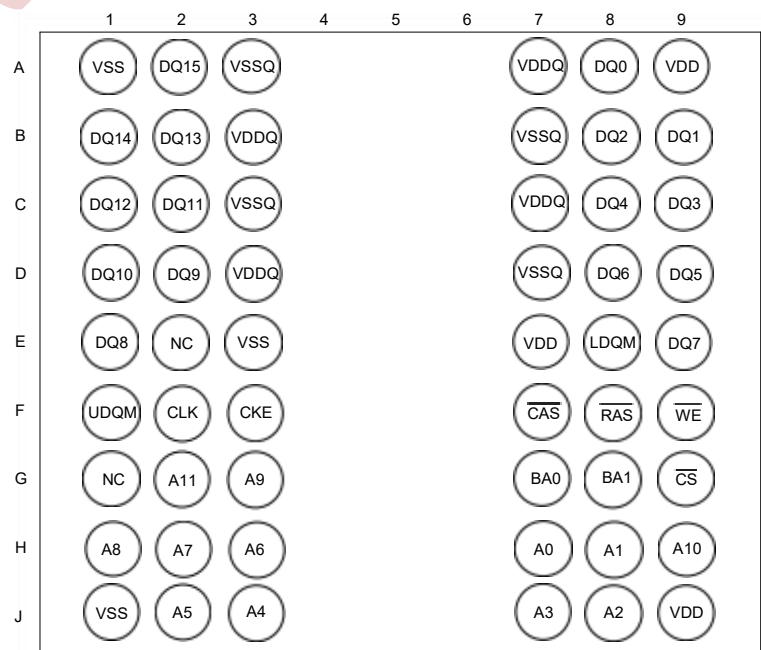
Product ID	Max Freq.	Package	Comments
CT51V4M1601A-5S	200MHz	54 TSOP II	Pb-free
CT51V4M1601A-6S	166MHz	54 TSOP II	Pb-free
CT51V4M1601A-7S	143MHz	54 TSOP II	Pb-free
CT51V4M1601A-5SI	200MHz	54 VBGA	Pb-free
CT51V4M1601A-6SI	166MHz	54 VBGA	Pb-free
CT51V4M1601A-7SI	143MHz	54 VBGA	Pb-free

PIN CONFIGURATION (TOP VIEW)

(TSOPII 54L, 400milX875mil Body, 0.8mm Pin Pitch)


BALL CONFIGURATION (TOP VIEW)

(BGA54, 8mmX8mmX1mm Body, 0.8mm Ball Pitch)



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Linda

