Features

- ⌘ JEDEC Standard
- ⌘ V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.8V ± 0.1V
- ⌘ Internal pipelined double-data-rate architecture; two data access per clock cycle
- ⌘ Bi-directional differential data strobe (DQS, DQS); DQS can be disabled for single-ended data strobe operation.
- ⌘ On-chip DLL
- ⌘ Differential clock inputs (CLK and CLK)
- ⌘ DLL aligns DQ and DQS transition with CLK transition
- ⌘ 8 bank operation
- ⌘ CAS Latency : 3, 4, 5, 6, 7
- ⌘ Additive Latency: 0, 1, 2, 3, 4, 5, 6
- ⌘ Burst Type : Sequential and Interleave
- ⌘ Burst Length : 4, 8
- ⌘ All inputs except data & DM are sampled at the rising edge of the system clock(CLK)
- ⌘ Data I/O transitions on both edges of data strobe (DQS)
- ⌘ DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- ⌘ Data mask (DM) for write masking only
- ⌘ Off-Chip-Driver (OCD) impedance adjustment
- ⌘ On-Die-Termination for better signal quality
- ⌘ Special function support
  - 50/ 75/ 150 ohm ODT
  - High Temperature Self refresh rate enable
  - Duty Cycle Corrector
- ⌘ Auto & Self refresh
- ⌘ Refresh cycle :
  - 8192 cycles/64ms (7.8μ s refresh interval) at 0 ℃ ≦ T_C ≦ +85 ℃
  - 8192 cycles/32ms (3.9μ s refresh interval) at +85 ℃ < T_C ≦ +95 ℃
- ⌘ SSTL_18 interface
- ⌘ If t_{CK} < 1.875ns, the device can not support Write with Auto Precharge function.

如需获取完整版规格书
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